

In The Claims:

1. An apparatus for testing a computer microarchitecture, comprising:
means for providing reprogrammed microcode, comprising:
means for reprogramming microcode;
5 means for storing reprogrammed microcode, comprising:
microcode related to one or more macroinstructions, and
reprogrammed test microcode for testing the computer
microarchitecture, wherein the reprogrammed test microcode comprises a
sequence of microinstructions executed to test the computer microarchitecture;
10 and
means for sequencing the sequence of microinstructions and producing an
address for the reprogrammed test microcode.
2. The apparatus of claim 1, further comprising:
a dispatcher that receives the sequence of microinstructions and provides outputs;
15 and
execution units that receive the outputs and execute microinstructions.
3. The apparatus of claim 1, wherein the computer microarchitecture supports
multiple instruction sets.
4. The apparatus of claim 1, wherein the apparatus is implemented as a software
20 model.
5. The apparatus of claim 4, wherein the software model is implemented on a
computer-readable medium.
6. The apparatus of claim 1, wherein the means for sequencing comprises a
macroinstruction to microinstruction mapper that maps macroinstructions into sequences
25 of microinstructions.
7. A method for testing a computer microarchitecture, comprising:
reprogramming microcode for storage in a microcode storage;
designating a macroinstruction for execution, wherein the execution initiates a test
sequence comprising the reprogrammed microcode;
30 receiving inputs corresponding to one or more of entry points and computer state
information; and
producing an address for the reprogrammed microcode.
8. The method of claim 7, further comprising:
providing the reprogrammed microcode to a dispatcher; and
35 dispatching the reprogrammed microcode to specified execution units for
execution of the microinstruction.
9. The method of claim 7, wherein the computer microarchitecture supports multiple
instruction sets.

10. A method for conducting a test of a computer microarchitecture, comprising:
mapping a macroinstruction to a particular sequence of microinstructions;
replacing the particular sequence of microinstructions with an arbitrary set of
microinstructions, wherein the arbitrary set of microinstructions comprises the test;
5 receiving inputs corresponding to one or more of entry points and computer state
information; and
producing an address for the arbitrary set of microinstructions.
11. The method of claim 10, wherein the computer microarchitecture supports
multiple instruction sets.
- 10 12. The method of claim 10, further comprising issuing the macroinstruction to
execute the test microinstructions.
13. A computer readable medium comprising code for conducting a test of a computer
microarchitecture, the code implementing the steps of:
mapping a macroinstruction to a particular sequence of microinstructions;
15 replacing the particular sequence of microinstructions with an arbitrary set of
microinstructions, wherein the arbitrary set of microinstructions comprises the test;
receiving inputs corresponding to one or more of entry points and computer state
information; and
producing an address for the arbitrary set of microinstructions.
- 20 14. The computer readable medium of claim 13, wherein the steps further comprise
issuing the microinstruction to execute the test microinstructions.